REMARKS

Claims 1-40 are all the claims pending in the application. Claims 14, 24 and 36-40 stand rejected under 35 U.S.C. §112, second paragraph. Claims 1-8 and 36-40 stand rejected under 35 U.S.C. §101. Claims 1-27 and 30-40 stand rejected on prior art grounds. Claim 33 is objected to. Claims 28 and 29 were not reexamined. Applicants respectfully traverse these rejections based on the following discussion.

I. Request For Withdrawal Of Premature Final Rejection.

37 C.F.R. §1.104(c)(2) provides that "In rejecting claims for want of novelty or for obviousness, the examiner must cite the best references at his or her command. When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified." Additionally, 37 C.F.R. §1.112 provides that "After reply by applicant ... to a non-final office action ..., the application or the patent under reexamination will be reconsidered and again examined. The applicant ... will be notified if claims are rejected, objections or requirements made, or decisions favorable to patentability are made, in the same manner as after the first examination (§1.104)." 37 C.F.R. § 1.113(b) provides that "In making such final rejection, the examiner shall repeat or state all grounds of rejection then considered applicable to the claims in the application, clearly stating the reasons in support thereof."

A. New Ground For Rejection Of Claim 23.

Regarding the rejection of independent claim 23, both the First Office Action on page 14 and the Final Office Action on page 19 state the following "Method claim 9 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1. HE'277 teaches determining a set of design distributions that are within a given set of performance targets for a plurality of parameters; altering different features of design; and determining whether altered design is within said set of design distributions. (HER'277: Col. 5 Line 63-Col. 4 Line 24)."

These are the only three method steps claimed in claim 23, none of which are claimed in claim 1 and furthermore claim 23 has not been amended. In response to the First Office Action, the Applicants' argued that, contrary to the Examiner's assertion, HE'277 did not address altering different features of the design, nor did it address altering different features of the design and then determining whether the altered design is within the set of design distributions. The Examiner responded in the Final Office Action by stating on page 7 that the "HE'277 reference is not used for this teaching. KR'527 teaches modifications to design wherein modification comprises modifying a particular feature ...". In summary:

(1) Claim 1 does not contain the same features that are claimed in claim 23.

(2) Claim 23 has not been amended.

(3) Page 14 of the First Office Action specifically stated that HE'277 was used for teaching all three of the claimed method steps.

(4) Page 19 of the Final Office Action also states that HE'277 teaches all three of the claimed method steps.

(5) Page 7 of the Final Office Action directly contradicts page 19, stating that HE'277 is not used for teaching these steps, but rather KR'527 is.

Therefore, the Applicants submit that this is a **new ground of rejection** that is neither necessitated by an amendment of the claim, nor based on information submitted in an information disclosure statement. Therefore, under §706.07(a) office action was not properly made final. Furthermore, even if the Examiner finds that this was not a new ground for rejection because the rejection of claim 1 was based on a combination of Hershenson and Krivokapic, the particular parts of each prior art reference that are relied are not designated, nor is the pertinence of each reference clearly explained (as evidenced by the contradictory statements within the Final Office Action itself). Thus, the requirements of 37 C.F.R. §1.104(c)(2) have not been met.

Therefore, under MPEP §706.07(d) the Applicants respectfully request that the primary examiner find that the final rejection was premature and withdraw the finality of the June 28, 2006 Office Action.

B. Claims 28 and 29 Not Re-examined.

Paragraph 3 of the Detailed Action rejects all claims stating that "Claims 1-40 remain rejected and this action is made Final." However, no where in the final office action does it reveal that Claims 28 and 29 were individually reconsidered and again examined, as required by 37 C.F.R. §1.112. Additionally, no wherein in the final office action does it cite the best

references for rejecting claims 28 and 29 at the Examiner's command, as required by §1.104, or repeat or state all grounds of rejection for claims 28 and 29, as required by §1.113.

Therefore, under MPEP §706.07(d) the Applicants respectfully request that the primary examiner find that the final rejection was premature and withdraw the finality of the June 28, 2006 Office Action.

C. Regarding claims 1, 9, 14, 19, 24, 36 and 40.

Regarding the rejection of independent claims 1, 9, 14, 19, 24, 36 and 40, the Office Action indicates that Hershenson does not teach "a first bounded range." Thus, the Office Action cites Krivokapic and states "Range bounds are also provided. (Abstract: lines 19-27 and Col. 8, lines 50-63). Since "range bounds" are not discussed in the cited portions and since the reference is complex and shows inventions other than that of the Applicants, the Applicants submit that pursuant to §1.104(c)(2), the particular part or feature that is relied on should have been designated as nearly as practicable and the pertinence clearly explained.

Therefore, under MPEP §706.07(d) the Applicants respectfully request that the primary examiner find that the final rejection was premature and withdraw the finality of the June 28, 2006 Office Action.

D. Regarding claim 9.

Regarding the rejection of independent claim 9, the Office Action simply states "Method claim 9 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1." However, independent claim 9 claims a computer-implemented method that comprises a

"designing" step using a computer model that is created using a given target performance parameter of a given performance attribute, which is a feature not included in the "simulator" of independent claim 1. Since the combined references cited are complex and describe inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable, under §1.104(c)(2).

Therefore, under MPEP §706.07(d) the Applicants respectfully request that the primary examiner find that the final rejection was premature and withdraw the finality of the June 28, 2006 Office Action.

II. Objection To Claim 33.

Claim 33 was previously objected to under 37 C.F.R. §1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim and the objection is maintained. Independent claim 30 is amended herein to remove the redundant feature of "correlating a secondary parameter to said primary parameter", leaving the feature of "calculating a secondary parameter based on said primary parameter". The feature in claim 33 of " wherein said calculating of said secondary parameter is performed using predetermined primary-to-secondary correlation calculations" further limits the calculating process in claim 30 by indicating the type of calculations to be used.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdrawal this rejection.

III. Rejection of Claims 14, 24 and 36-40 under 35 U.S.C. §112, second paragraph.

Claims 14, 24 and 36-40 stand rejected under 35 U.S.C. §112, second paragraph. These rejections are traversed as explained below.

A. Regarding Claims 14 and 24.

The Examiner previously rejected claim 14 based on the following "Claim 14 discloses a method of "developing a product having a device" including a step of "producing a target model". If "developing" is understood as conceptual representation of the actual device (not a real manufactured device), claim does not provide any difference between the product, device and target model. Further, no distinction provided between product and device, clarifying how their designing is different from each other. Else if "developing" is understood as producing a actual product (and/or device-distinction unclear) than the target model is clearly a conceptual representation and product is a real semiconductor ship (for example). Since various interpretation of terms "developing, product, device, target model" are possible this claim is vague and indefinite, limiting one of ordinary skill in the art for making/practicing the invention."

The Applicants traversed this rejection, amending the claims and providing support within the specification, to clarify the terms which the Examiner indicates are vague and indefinite. The Applicants again traverse this rejection based on the following discussion and also amend claim 14 to further clarify the terms and there relationship to each other.

More particularly, when rejecting a claim under 35 U.S.C. §112, ¶2, the "[d]efiniteness of claim language is analyzed, not in a vacuum, but always in light of the teachings of the prior art and **of the particular application disclosure** as it would be interpreted by one possessing the

ordinary level of skill in the pertinent art." (see In re Moore, 439 F.2d 1232, 169 USPQ 236 (CCPA 1971). See also MPEP 2173.02). Furthermore, "The definiteness of claim language must also be analyzed **in light of the claim interpretation that would be given by one possessing the ordinary level of skill in the pertinent art at the time the invention was made**. W. L. Gore & Assoc., Inc. v. Garlock, Inc., 220 USPQ 303 (Fed. Cir. 1983). Given the standard set forth above, the Applicants submit that if the claim language were analyzed based on both the teachings of the prior art and on the information disclosed in the present application, it would be considered by one with an ordinary skill in the art to be definite.

Specifically, the method of claim 14 is "A method of developing a product having a device." Please refer to paragraph [0017] of published patent application US 2003/0114944 A1 of the detailed description section of the specification that states the following:

> [0017] In the description to follow, reference will be made to "devices" and "products". In the preferred embodiment, "device" refers to an active or passive integrated circuit component, such as a transistor, capacitor, resistor, or the like (most preferably, it refers to a transistor), and "product" refers to the overall integrated circuit chip. However, it is to be understood that the invention is also applicable to any component of any product, where the performance attributes of that component help determine the functionality of the integrated product. Examples include chemical components and subcomponents of a drug, or the insole of a shoe, or the foam insulation of a hot tub. In each example, the former is the "device" and the latter is the "product".

Consequently, in light of paragraph [0017], the method would include a method of developing an integrated circuit (i.e., a product) having a component, such as a transistor, capacitor, resistor, or the like (i.e., a device).

The Office Action indicates that this paragraph [0017] was pointed to by the Applicant "rather confusingly, to clarify the distinction between product and device" and the Examiner further asserts "the specification paragraph [0017] does not even disclose a produce." However, given the direct quote from specification paragraph [0017], "In the preferred embodiment, "device" refers to an active or passive integrated circuit component, such as a transistor, capacitor, resistor, or the like (most preferably, it refers to a transistor), and "product" refers to the overall integrated circuit chip", it appears that the Examiner may have mistakenly looked at a different paragraph; hence, the confusion.

Please refer to Figure 4 and paragraphs [0032-0035] of the specification which describe in detail the method of the present invention as claimed in claim 14.

Specifically, paragraph [0032] provides that the device (i.e., the single IC component, see paragraph [0017]) design starts at item 400 and the circuit (i.e., the product, see paragraph [0017]) design starts at item 430. Product goals are developed (see item 432). Then, device goals (i.e., conceptual objectives that the device should achieve) are developed based at least in part on the product goals (see item 402). From these goals, target performance parameters are developed (see item 404) for the device, as described in paragraph [0033]. That is, a particular cost/performance point will be targeted for the device see paragraph [0019]), which is expressed within a range (see paragraph [0020]).

Paragraph [0034] provides that a target model (i.e., a computer model that is intended to be predictive of the final process performance of the device (see paragraph [0007]) is created using the target performance parameters and the device goals. A "target model 406 is a set of equations (typically embodied in a set of software subroutines that are part of a circuit network

simulation program)" (see paragraph [0047]). Once a target model is completed, it is made available to the circuit (i.e., the product, see paragraph [0017]) designers.

Paragraph [0035] provides that the circuit (i.e., the product, see paragraph [0017]) design process relies upon the target performance parameters and the target model to create a circuit model of the chip (i.e., of the product, see paragraph [0017]). This circuit model is then simulated and the results of the simulation are checked to determine whether the circuit goals have been met. If the circuit goals have been met, the circuit (i.e., the product including the device) is physically produced and tested.

Given the detailed description of the method provided in the specification and the fact that the language of the claims must always be viewed in light of the teachings of the prior art and **of the particular application disclosure** as it would be interpreted by one possessing the ordinary level of skill in the pertinent art, the Applicants assert that there is nothing vague or indefinite about the features in amended independent claims 14 and 24.

B. Regarding Claims 36-40

Claims 36-40 were rejected because independent claims 36 and 40 recites a set of subroutines created using a target performance parameter for said performance attribute and, according to the Examiner, it is unclear what functional step the subroutines are performing. Claims 36 amended herein to include the feature of "wherein said set of subroutines, when executed, predict process and design variations of said device," and claim 40 is amended hereinto include the feature of "wherein said target model comprises a set of subroutines that are adapted to predict process and design variations of said device" (see paragraphs [0034], [0004], and [0047].

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection of claims 36-40.

IV. Rejection of Claims 1-8 and 36-40 under 35 U.S.C. §101

Claims 1-8 and 36-40 stand rejected under 35 U.S.C. §101 because the claimed invention is directed to non-statutory subject matter. These rejections are traversed as explained below.

A. Regarding Claims 1-8

Claims 1-8 stands rejected under 35 U.S.C. §101 because independent claim 1 was directed towards non-statutory subject matter. That is, the Office Action indicated that "a simulator merely having a computer model of an integrated circuit, does not perform any function, thereby does not claim a method or process" and that no "discrete physical structure or materials are recited hence that precludes other machines, manufactures or compositions of matter categories." In order to overcome this rejection, claim 1 is amended herein to include "a **memory** for storing a computer model of an integrated circuit comprising a device that is one of a transistor, a capacitor and a resistor and that has at least one performance attribute, wherein said computer model is generated based on a target model for said transistor and wherein said target model is created using a target performance parameter for said performance attribute and is adapted to predict process and design variations of said device; **and a processor** in communication with said memory device and adapted to execute said computer model" (see paragraphs [0034], [0004], and [0047-0049]. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection of claims 1-8.

B. Regarding Claims 36-39

Claims 36-39 were rejected because independent claim 36 was drawn to non-statutory descriptive material since the claimed computer readable medium storing a computer model do not appear to impart any functionality (i.e., not a computer program product or executable instructions embodied on a computer readable medium). In order to overcome this rejection, claim 36 is amended herein to include "A program storage device readable by computer and tangibly embodying a computer model of an integrated circuit device that has at least one performance attribute and that is executable by said computer, said model comprising: a set of software subroutines created using a target performance parameter for said performance attribute, wherein said set of subroutines, when executed by said computer, predict process and design variations of said device". In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection of claims 36-39.

C. Regarding Claim 40

Independent claim 40 was rejected because, as written, it was drawn to nonstatutory descriptive material under the same rationale cited for claim 36. In order to overcome this rejection, claim 40 is amended herein to include "A program storage device readable by computer and tangibly embodying a program of instructions executable by said computer to perform an integrated circuit development method, said method comprising: producing a target model of a device for a product using a target performance parameter for a performance attribute of said device, wherein said device is one of a transistor, a capacitor and a resistor, and wherein said target model comprises a set of that are adapted to predict process and design variations of said device, ...and creating a computer model of said product, wherein said computer model of

said product is based on said target model." (see paragraphs [0032-0035], [0004], and [0047-0049]). In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection of claim 40.

V. Rejection of Claims 1-27 and 30-40 under 35 U.S.C. §103(a)

Claims 1-27 and 30-40 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hershenson, et al. (U.S. Patent No. 6,269,277) hereinafter referred to as Hershenson, in view of Krivokapic, et al. (U.S. Patent No. 5,966,527), hereinafter referred to as Krivokapic. Applicants respectfully traverse these rejections based on the following discussion.

A. Regarding independent claims 1, 9, 14, 19, 24, 36 and 40.

The Applicants submit that neither Hershenson, nor Krivokapic teach or suggest the following features of independent claims 1, 9, 14, 19, 24, 36 and 40:

"wherein said target model is created using a target performance parameter for said performance attribute and is adapted to predict process and design variations of said device;

"wherein said target performance parameter includes a first bounded range and a second bounded range,"

"wherein said first bounded range comprises performance parameter variations within a single manufacturing process based on a single design for said device," and

"wherein said second bounded range comprises performance parameter variations between multiple designs for said device."

Hershenson provides a system for designing integrated circuits in a manner different from the present invention. Specifically, referring to col. 5, line 35-col. 6, line 25, Hershenson

provides that when a new semiconductor manufacturing process is initiated on the CAD system, models for the transistors (i.e., a single component of an IC) are generated. The CAD system may include posynomial models of different levels and complexity that can be selected as needed based on the design requirements. The CAD system also includes a library of circuit topologies. Topologies are generally understood to be configurations (i.e., a relative arrangements of components, parts or elements (see Merriam-Webster Online Dictionary copyright © 2005 by Merriam-Webster, Incorporated). The library is divided into groups based on multi-component device type (e.g., op-amps, amplifiers for automatic gain control, limiters, oscillators, etc.). Thus, it is understood that the library includes, for each multi-component device, one or more different topologies or different relative arrangements of the individual components (e.g., transistors) within the devices.

After a transistor model is selected, a user selects a circuit topology or group of circuit topologies for the device from the library and then selects performance specifications for the desired device (i.e., for the desired op-amp, oscillator, etc.). More specifically, for a given multi-component device (e.g., an op-amp) the user determines the design parameters and performance specifications (see col. 10, line 35-col. 11, line 30). Each performance specification is defined in posynomial form for use in a geometric program. The system then generates a geometric program for the defined performance specification of the multi-component device, and based on a user-selected optimization mode, reformulates the geometric program as convex optimizations problems (see col. 7, lines 60-67). The program solves the geometric program for the desired results.

The Office Action cites col. 4, Lines 5-26 of Hershenson as disclosing a performance parameter includes a first bounded range and a second bounded range as "inequality constraints." The Applicants respectfully disagree. More specifically, the performance specifications referred to Hershenson are directed specifically to the overall performance specifications for a multi-component device such as an op-amp, etc. that includes several transistors, not to the performance specifications for each individual transistor within the multi-component device. Additionally, the cited portion of Hershenson provides "One embodiment reformulates geometric programs as convex optimization problems, i.e., the problem of minimizing a convex function subject to convex inequalities constraints and linear equality constraints ...". However, as discussed in col. 11 lines 41-65 of Hershenson, equality constraints refer to identical conditions between different transistors within the multi-component device and, as discussed in col. 13, line 5-col. 14 line 25, inequality constraints refer to non-identical conditions between different transistors within the multi-component device. Thus, these inequality constraints do not amount to a first bounded range or a second bounded range of a performance parameter of a single component device (e.g., a transistor, capacitor or a resistor).

The Office Action provides that the feature of "wherein said second bounded range comprises performance parameter variations between multiple designs" is disclosed as "various device topologies", citing col. 3, lines 62-67, col. 5 lines 40-46, 50-67 and col. 6, lines 1-2. These various device topologies simply refer to different component configurations for multi-component devices, such as op-amps or oscillators, not to a second bounded range that comprises performance parameter variations between multiple designs for a single component (i.e., a transistor, a capacitor or a resistor) within one of the circuit topologies.

The Office Action further admits that Hershenson does not teach the "first bounded range comprising performance parameter variations within a single manufacturing process." Thus, the Office Action cites element 620a of Figure 6a of Krivokapic as teaching a semiconductor process simulator, elements 602a-e of Figure 6a of Krivokapic as teaching process parameters for individual processes Figure 6a-6b, and elements 690, 693-695 to indicate that the process parameters "are sampled in and or simulated from the Monte Carlo Engine..." The Office Action further provides that "Range bounds are also provided (Abstract: Lines 19-27; Col. 8, lines 50-63) and that it would have been obvious to one of ordinary skill in the art to apply the teachings of Krivokapic to Hershenson.

However, no where in the cited portions of Krivokapic are "range bounds" of target performance parameters disclosed. More particularly, Krivokapic first discloses a prior art method for modeling, in particular to obtain I/V curves for a transistor having specified attributes (see Figure 1 and the associated text). It then indicates that the prior art method for modeling suffers from disadvantages because due to the fact that the parameters (e.g., physical measurements (see col. 2, lines 50-65)) do not accurately reflect mass-produced semiconductor devices, the I/V curve and five corners do not reflect realistic worst-case curves and device envelopes, respectively (see col. 3, lines 42-48). Additionally, prior methods do not use semiconductor manufacturing process simulations to generate distributions of manufactured semiconductor devices (see col. 3, line 66- col. 4, line 3). Thus, Krivokapic discloses an improved method for modeling in which the I/V curves that are obtained are used to show how choice of semiconductor device attributes, such as channel length, effect the guard band or manufacturability of such devices (see col. 4, lines 26-34).

The cited portions of Krivokapic refer to these I/V curves that "are obtained from the modeling" and to the guard bands. Therefore, the Applicants have assumed for the sake of argument that these I/V curves and/or guard bands are what the Office Action is referring to as "range bounds." Specifically, simulated mass-produced devices are input into a device simulator to obtain I/V curves. Worst-case I/V curves are obtained and parameters for the device simulator are extracted from these worst-case I/V curves. Worst-case I/V curves can also be compared to an ideal I/V curve to obtain manufacturing guard bands (see col. 9, lines 35-60). Thus, the cited portions of Krivokapic do not amount to a first bounded range of a target performance parameter for a performance attribute, where the performance parameter variations occur within a single manufacturing process and where the target performance parameter is used "to create" a target model. Rather, the I/V curves and, in particular, the guard bands are "obtained from" the modeling not used to create a model.

It should also be noted that the Office Action has indicated that theses I/V curves teach a completely different and patentable feature set out in claim 19, namely, the secondary parameters (see discussion regarding claim 19 below).

Therefore, independent claims 1, 9, 14, 19, 24, 36 and 40 are patentable over Hershenson in combination with Krivokapic. Furthermore, dependent claims 2-8, 10-13, 15-18, 20-22, 25-35, and 37-39 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

B. Regarding the rejection of independent claims 1, 24 and 40

The Applicant's further submit that neither Hershenson, nor Krivokapic teach or suggest the following additional features of independent claims 1, 24 and 40: (1) that the computer model (of an integrated circuit or product having a device) is generated based on a target model for the device (i.e., a target model for the transistor, resistor or capacitor) within the product or integrated circuit or (2) that the target model is created using a target performance parameter for a performance attribute of the device.

As mentioned above, in Hereshenson, after a transistor model is selected, a user selects a circuit topology or group of circuit topologies for the device from the library and then selects performance specifications for the desired device (i.e., for the desired op-amp, oscillator, etc.). More specifically, for a given multi-component device (e.g., an op-amp) the user determines the design parameters and performance specifications (see col. 10, line 35-col. 11, line 30). Each performance specification is defined in posynomial form for use in a geometric program. The system then generates a geometric program for the defined performance specification of the multi-component device, and based on a user-selected optimization mode, reformulates the geometric program as convex optimizations problems (see col. 7, lines 60-67). The program solves the geometric program for the desired results. Thus, in Hershenson, a generic transistor model based on design considerations without reference to specific target performance attributes at the transistor level (i.e., without a "target model" for the transistor). Then, a geometric program is optimized at the multi-component (i.e., product) level based on target performance attributes for the multi-component device. Thus, Hereshenson does not disclose a computer model for an IC (or product) that is based on a target model which in turn is based on a performance parameter for a given device (e.g., transistor, capacitor, or resistor) within the IC (or

product), but rather an optimized geometric program that is based on both a transistor model (without additional details) and performance specifications for the multi-component device.

Therefore, independent claims 1, 24 and 40 are patentable over Hershenson in combination with Krivokapic. Furthermore, dependent claims 2-8 and 25-35 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

C. Rejection of independent claim 19.

In additional to the features described above with regard to claim 19, the cited prior art also does not teach or suggest the following features: (1) "determining primary parameters for said particular feature;" (2) "determining secondary parameters from said primary parameters;" (3) "proposing a modification of the design that comprises either adding a particular feature into the design or modifying an already present feature; and (4) "balancing design choices related to said modification and, particularly, to said primary parameters and said secondary parameters in order to maintain device performance within said first bounded range and said second bounded range of said target performance parameter."

More specifically, the Office Action states that "Proposed feature is understood as performance parameter having first bound (primary parameter) and second bound (secondary parameter)." This meaning of this statement is unclear. First and second bounds are not features of the claimed invention. The target performance parameter, as claimed, does include a first bounded range and a second bounded range. However, it does not make sense for the Examiner to conclude that the primary parameter is somehow the equivalent of the first bounded range or

that the secondary parameter is somehow the equivalent of the second bounded range. That is, as claimed the "primary parameters" relate to a particular feature that is either added to or modified in a design, which was previously developed based on a target model. The target model in turn was created using a target performance parameter that includes the first bounded range and the second bounded range. (Note that paragraphs [0040-0043] of the specification provide a detailed explanation of the correlation between the primary and secondary parameters). Thus, the first and second bounded ranges and the primary and secondary parameters are completely different patentable features of the invention.

However, it appears that the Examiner is indicating that these I/Vcurves amount to the first bounded range of the target performance parameters that are used to create a target model and, thereby, a device design and that these I/V curves also amount to the secondary parameters which are based on primary parameters of a feature that was subsequently added to or modified within the device design. As the features first and second bounded ranges and primary and secondary parameters are completely different, the same feature of Krivokapic can not teach them both.

Therefore, independent claim 19 is further patentable over Hershenson in combination with Krivokapic. Furthermore, dependent claims 20-22 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

D. Rejection of independent claim 23.

On page 19 of the Final Office Action, the Examiner indicates that claim 23 discloses

similar limitations as claim 1 and that it is rejected for the same reasons as claim 1. Additionally, citing Hershenson col. 5, line 63- col. 6, line 24, the Final Office Action indicates that Hershenson teaches each three claimed method steps. However, page 7 of the Final Office Action also states that "HE'277 reference is not used for this teaching. KR'527 teaches modifications to design wherein modification comprises modifying a particular feature ...". The portions of KR '527 cited by the Final Office Action and the discussion related thereto, do not address each of claim limitations contained in claim 23, but rather appear to address features contained claim 19 (e.g., modifying a particular feature, balancing choices, etc.).

No wherein in the cited prior art does it disclose "determining a set of design distributions that are within a given set of performance targets for a plurality of parameters" and then determining whether an altered design is within "said set of design distributions". As discussed in detail above, the I/V curves and guard bands of Krivokapic are determined by actual device measurements and are not, therefore, "a set of design distributions that are within a set of performance targets of a plurality of parameters."

Therefore, independent claim 23 is patentable over Hershenson in combination with Krivokapic. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

D. Rejection of all claims.

The Applicants further assert that prima facie obviousness has not been established to reject any of the claims based on a combination of both Hershenson and Krivokapic because these prior art references fail to either explicitly or implicitly provide some teaching, suggestion, or motivation to combine. Specifically, MPEP§ 2143.01 provides that "Obviousness can only be

established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art." The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." *In re Kotzab,* 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). Specifically, Hershenson discloses a system for designing and optimizing integrated circuits. The design objectives and constraints are described as a posynomial function of the design parameters in order to achieve globally optimal circuit designs for a given circuit topology library (see Abstract), prior to fabrication. Contrarily, Krivokapic teaches a monitoring and correction system for a single fabrication line (see col. 9, lines 62-63, Figures 6a-b) as well as an associated method for modeling mass-produced semiconductor devices to obtain I/V curves from actually measured samples from that fabrication line (col. 4, lines 25-33). Thus, the different natures of the problems to be solved, combining the references would not have been obvious. That is, Hershenson, like the present invention albeit in a different manner, uses modeling to design a globally optimal integrated circuit. Thus, preventing the need for corrections during manufacturing. Whereas, Krivokapic provides a modeling method that allows for process/design corrections during manufacturing.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejection of all claims based on Hershenson in view of Krivokapic.

VI. Formal Matters and Conclusion

In view of the foregoing, the Examiner is respectfully requested to withdrawal the finality of June 28, 2006 Office Action and enter the claim amendments submitted herewith. With respect to the objections to the claims, the claims have been amended, above, to overcome these objections. Similarly, with respect to the rejections to the claims, the claims have been amended, above, to overcome these rejections. Moreover, the Applicants note that all claims are properly supported in the specification and accompanying drawings, and no new matter is being added.

In view of the foregoing, Applicants submit that claims 1-40, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance and the Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: 8/15/06

Pamela M. Riley, Esq.
Registration No. 40,146

Gibb I.P. Law Firm, LLC
2568-A Riva Road, Suite 304
Annapolis, MD 21401
Voice: (410) 573-0227
Fax: (301) 261-8825
Customer Number: 29154